LISTING OF CLAIMS:

The following listing of claims replaces all previous versions and listings.

Please cancel claims 1-13 without prejudice or disclaimer due to restriction.

Please cancel claim 14.

1. – 13. (Canceled)

14. (Canceled)

15. (Currently amended) The method according to claim ~~14~~ 38, wherein the semiconductor substrate, in a region of which the diffusion structure is formed, is a silicon on insulator substrate.

16. (Original) The method according to claim 15, wherein:

the silicon on insulator substrate includes a semiconductor layer formed on an insulating layer; and

the semiconductor layer is equal to or less than five micrometers.

17. (Currently amended) The method according to claim ~~14~~ 38, further comprising filling in the trench with borophosphosilicate glass.

18. (Currently amended) The method according to claim ~~14~~ 38, wherein the diffusion structure is formed including a repeated pattern in the region.

19. (Currently amended) The method according to claim ~~14~~ 38, wherein the diffusion structure is formed including diffusion regions shaped in a rectangular.

20. (Currently amended) The method according to claim ~~14~~ 38, wherein the semiconductor component formed in the separating step is an analog component for processing an analog signal.

21. (Original) The method according to claim 20, wherein the analog component is a bipolar transistor.

22. (Currently amended) The method according to claim ~~14~~ 38, wherein the semiconductor component formed in the separating step is a power component for controlling power supply.

23. (Withdrawn) The method according to claim 22, wherein the power component is an insulated gate bipolar transistor.

24. (Original) The method according to claim 22, wherein the power component is an LDMOS transistor.

25. (Currently amended) The method according to claim ~~14~~ 38, wherein the semiconductor device manufactured by the method is a hybrid IC including different kinds of semiconductor components integrated into a single chip.

26. (Original) A method for manufacturing a semiconductor device that includes a plurality of semiconductor components of a kind in a region of a semiconductor substrate, comprising:

forming a common diffusion structure in the region in which the semiconductor components are formed;

separating parts of the diffusion structure from a surrounding area thereof by trenches to form the semiconductor components along with defining sizes of the semiconductor components; and

connecting metallization patterns to the semiconductor components.

27. (Original) The method according to claim 26, wherein the semiconductor substrate, in a region of which the diffusion structure is formed, is a silicon on insulator substrate.

28. (Original) The method according to claim 27, wherein:

the silicon on insulator substrate includes a semiconductor layer formed on an insulating layer; and

the semiconductor layer is equal to or less than five micrometers.

29. (Original) The method according to claim 26, further comprising filling in the trench with borophosphosilicate glass.

30. (Original) The method according to claim 26, wherein the diffusion structure is formed including a repeated pattern in the region.

31. (Original) The method according to claim 26, wherein the diffusion structure is formed including diffusion regions shaped in a rectangular.

32. (Previously presented) The method according to claim 26, wherein the semiconductor component formed in separating step is an analog component for processing an analog signal.

33. (Original) The method according to claim 32, wherein the analog component is a bipolar transistor.

34. (Previously presented) The method according to claim 26, wherein the semiconductor component formed in separating step is a power component for controlling power supply.

35. (Withdrawn) The method according to claim 34, wherein the power component is an insulated gate bipolar transistor.

36. (Original) The method according to claim 34, wherein the power component is an LDMOS transistor.

37. (Previously presented) The method according to claim 26, wherein the semiconductor device includes a hybrid IC and wherein the plurality of semiconductor components are integrated into a single chip.

38. (Previously presented) A method for manufacturing a semiconductor device that includes a semiconductor component of a kind formed in a substrate, the method comprising:

forming a diffusion structure including a repeated pattern of diffusion regions common to the kind in an area of the substrate, in which the semiconductor component is to be formed;

separating a part of the diffusion structure from a surrounding area thereof by forming a trench for encircling the part of the diffusion structure including at least a part of the repeated pattern of diffusion regions so as to define the semiconductor component including a predetermined size thereof, and to insulate the semiconductor component from the surrounding area after forming the diffusion structure; and

connecting a metallization pattern to the semiconductor component.

39. (Previously presented) A method for manufacturing a semiconductor device that includes a first semiconductor component and a second semiconductor component formed in a substrate, the method comprising:

forming a first diffusion structure including a first repeated pattern of first diffusion regions common to a first kind in a first area of the substrate in which the first semiconductor component is to be formed;

forming a second diffusion structure including a second repeated pattern of second diffusion regions common to a second kind in a second area of the substrate in which the second semiconductor component is to be formed;

separating a part of the first diffusion structure from a surrounding area thereof by forming a first closed trench for encircling at least a part of the first diffusion structure including at least a part of the first repeated pattern of the first diffusion regions to define the first semiconductor component of the first kind including a first predetermined size thereof, and to insulate the first semiconductor component from the surrounding area after forming the first

diffusion structure and by connecting a first metallization pattern to the first semiconductor component; and

separating a part of the second diffusion structure from the surrounding area by forming a second closed trench for encircling at least a part of the second diffusion structure including at least a part of the second repeated pattern of the second diffusion regions to define the second semiconductor component of the second kind including a second predetermined size thereof, and to insulate the second semiconductor component from the surrounding area after forming the second diffusion structure and by connecting a second metallization pattern to the second semiconductor component.

40. (Previously presented) A method for manufacturing a semiconductor device that includes a semiconductor component of one of a plurality of kinds formed in a substrate, the method comprising:

forming a plurality of diffusion structures associated with the plurality of kinds, each of the plurality of diffusion structures including a repeated pattern of diffusion regions common to one of the plurality of kinds, in an area of the substrate, in which the semiconductor component of the one of the plurality of kinds is formed;

separating a part of one of the plurality of diffusion structures from a surrounding area thereof by forming a trench, which encircles the part of the one of the plurality of diffusion structures including at least a part of the repeated pattern of the diffusion regions to define the semiconductor component of the one of the plurality of kinds including a predetermined size thereof, and to insulate the semiconductor component from the surrounding area, after forming the diffusion structures; and

connecting metallization patterns to the semiconductor component.